WHAT IS CLAIMED IS:

1. A method of testing an integrated circuit comprising:

receiving test output data from a circuit-under-test;

delaying the test output data;

comparing the test output data with the delayed test output data to generate a first compare signal;

generating a control signal; and

comparing the control signal to the first compare signal to generate a second compare signal.

2. The method of claim 1 further comprising:

if the second compare signal toggles from a first state to a second state while receiving the test output data; then

providing a signal indicating an error; else

providing a signal indicating no error.

3. The method of claim 1 further comprising:

changing the control signal such that the second compare signal toggles from the first state to the second state.

4. The method of claim 1 further comprising:

toggling the control signal when the test output data is expected to toggle.

5. The method of claim 3 further comprising:

after changing the control signal such that the second compare signal toggles from the first state to the second state;

providing a signal indicating an error.

6. The method of claim 1 further comprising:

after receiving test output data from a circuit-under-test; and

retiming the test output data to a clock signal, the clock signal comprising a plurality of clock cycles.

7. The method of claim 6 wherein the test output data is delayed one clock cycle.

8. The method of claim 1 wherein the delay is done using a flip-flop.

9. The method of claim 1 wherein the test output data and the delayed test output data are retimed to a clock signal, the clock signal comprising a plurality of clock cycles.

10. The method of claim 9 wherein the retiming circuits are preloaded with expected data to generate a first compare signal.

11. The method of claim 8 wherein the comparing the test output data with the delayed test output data to generate a first compare signal and comparing the control signal to the first compare signal to generate a second compare signal are done using a first exclusive-OR gate and a second exclusive-OR gate.

12. An integrated circuit comprising:

a delay circuit;

a first compare circuit coupled to the delay circuit; and

a second compare circuit coupled to the first compare circuit and further coupled to receive a control signal.

13. The integrated circuit of claim 12 further comprising:

a retiming circuit coupled to the delay circuit.

14. The integrated circuit of claim 13 further comprising:

a state machine coupled to the second compare circuit.

15. The integrated circuit of claim 12 wherein the first compare circuit and the second compare circuit are exclusive-OR gates.

16. The integrated circuit of claim 12 wherein the integrated circuit is a field programmable logic device further comprising:

a plurality of logic elements coupled by a plurality of programmable interconnect lines.

17. The integrated circuit of claim 16 further comprising:

an error memory circuit coupled to the second compare circuit.

18. An integrated circuit comprising:

a series combination including a retiming circuit in series with a delay circuit, wherein the retiming circuit is configured to retime test data to a clock signal and the delay circuit is configured to delay the test data;

a first compare circuit coupled to receive an output of the series combination;

a second compare circuit coupled to receive an output of the first compare circuit, and further coupled to receive a control signal.

19. The integrated circuit of claim 18 wherein the delay circuit has an input coupled to an output of the retiming circuit.

20. The integrated circuit of claim 18 wherein a state machine is configured to provide the control signal.

21. The integrated circuit of claim 20 further comprising a second retiming circuit configured to retime the test data and provide an output to the first compare circuit.

22. The integrated circuit of claim 18wherein the first compare circuit and the second compare circuit are exclusive-OR gates.

23. The integrated circuit of claim 18 wherein the integrated circuit is a field programmable logic device further comprising:

a plurality of logic elements coupled by a plurality of programmable interconnect lines.

24. The integrated circuit of claim 18 wherein the error circuit comprises an OR gate having an output coupled to an input of a flip-flop, the OR gate configured to receive an output from the flip-flop and the output from the second compare circuit.

25 The integrated circuit of claim 24 further comprising:

a error circuit coupled to receive an output of the second compare circuit.